Tracking Performance and Radiation Tolerance of Monolithic Active Pixel Sensors

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Abstract

CMOS sensors are being developed at IReS-LEPSI since 3 years in perspective of future vertex detectors needing very high granularity and minimal material budget. The first prototypes, made of small arrays of a few thousands of pixels, demonstrated the viability of the technology and its high tracking performances (e.g. signal-to-noise ratio = 20-30, more than 99% detection efficiency, spatial resolution of 1.5 μm). As a consequence, CMOS sensors are now being considered as promising alternatives to existing technologies for various vertex detectors of the coming decade, as well as for numerous other applications in various fields.

Important steps were achieved recently in order to further understand the characteristics of this new technology and to continue assessing it for its different application domains: the radiation tolerance of sensors to high neutron fluences were studied and a real scale prototype, made of arrays of 1 million of pixels, was fabricated. Preliminary results on radiation tolerance and on the performances of the real scale prototype are presented.

Keywords: CMOS active pixel sensors ; vertex detectors ; radiation hardness

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1. Introduction

The ability of Monolithic Active Pixel Sensors (MAPS), realized in a standard CMOS process, to provide charge particle tracking has been demonstrated on a series of MIMOSA (standing for Minimum Ionizing MOS Active sensor) chip prototypes [1,2]. The key element is the use of an n-well/p-epi diode to collect, through thermal diffusion, the charge generated by the impinging particle in the thin epitaxial layer underneath the readout electronics [3]. The measured tracking performances achieved with the first prototypes are very high: a spatial resolution of 1.5 μm and detection efficiency close to 100%. This results from a high signal-to-noise (S/N) ratio. The excellent tracking performances observed make CMOS APS a technology suitable for vertex detectors of future linear collider experiments [4]. New prototypes were produced since, which allowed to further investigate the properties of this technology and to make new steps towards real scale units.

2. The first prototypes

Since 1999, five generations of CMOS MAPS were designed and successfully tested by IReS-LEPSI collaboration. The first prototypes were small matrices of a classic three MOS transistors design, with an n-well/p-epi diode as a charge collecting element. The principle of operation and the prototype design are described in detail elsewhere [1,2]. Different CMOS processes were used to fabricate the chips in order to investigate the influence of the technology on their properties: the feature size ranged from 0.6 μm (MIMOSA I) to 0.25 μm (MIMOSA III). All the chips were arranged in a form containing 4 to 6 independent arrays of pixels having slightly different designs. The number of active elements in each array was 64x64 with a pitch of 20 μm in the case of MIMOSA I, II, and IV, and 128x128 pixels with a pitch of 8 μm in the MIMOSA III prototype. The goal of the first two prototypes was to demonstrate the adequacy of this new technique for charge particle detection. The design of MIMOSA III and IV allowed to test several specific features: the possibility to use deep sub-micron processes (i.e. with a thin epitaxial layer or processes without epitaxial layer), radiation tolerant and low noise designs, alternative charge sensing elements etc. All MIMOSA chips are equipped with a serial analogue read-out, requiring, apart of a few lines used to bias the circuitry, only two digital signals to operate.

The prototypes were tested with 120 GeV/c π^- beam at the CERN SPS. A precise reference detector provided the position of the beam particle within the aperture of a chip under test with an accuracy of ~1 μm. The MIMOSA spatial resolution was derived by comparing the track impact predicted by the reference detector to the result of a cluster centroid calculation based on the chip signal. For MIMOSA I and II the spatial resolution was found to be ~1.5μm and ~2μm respectively. The spatial resolution is mainly determined by the pixel pitch and by the charge spread which depends on the thickness of the sensitive volume. For the first 3 prototypes, the sensitive volume is essentially the epitaxial layer, while it is the substrate in the case of MIMOSA IV, which was fabricated without epitaxial layer but with a low doping substrate. This leads to substantially wider charge distribution in clusters and therefore to some deterioration in spatial resolution (measured to be ~ 4 μm) for the given pixel pitch. Nevertheless the detection efficiency is close to 100% and the average value of S/N is ~28. The performances of this prototype show that this alternative manufacturing process may also be adequate for charge particle tracking.

2.1. Double hit resolution

The track density in vertex detectors can be very high, especially in the layers closest to the interaction point. The double track resolution was investigated with the test beam data. Real individual clusters were brought together step by step and the separation efficiency of the two clusters was measured for 100μm (where clusters never overlap) to ~0 μm (where they fully overlap). Making use of the cluster charge distribution the double hit clusters were approximated either by a single cluster distribution or by a sum of two clusters. One of the hypotheses was chosen in accordance with the quality of the fit. It was found that above a distance of ~30 µm two neighboring clusters are fully reconstructed preserving the spatial resolution for the individual hit position.

2.2. Radiation tolerance of the first prototypes

The very high reaction rate and the beam induced background expected in future experiments set several requirements on the radiation hardness of basic detector components. This is particularly true for vertex detectors, because of their location close to the interaction point. Radiation damage may be induced by direct ionization due to the interaction of charged particles or energetic photons, followed by positive charge built-up in the oxide close to silicon interfaces. Heavy interacting particles (e.g. neutrons or protons) may also induce atom displacement in the silicon crystal lattice (bulk damage).

The sensitivity of MAPS to neutron irradiation was investigated using the MIMOSA I and II prototypes with different pixel layouts. Tests were performed with chips irradiated with fast neutrons (with an energy distribution peaked around 1 MeV) at reactors in JINR (Dubna) and via the CEA-Saclay. Several parameters were scrutinized. The charge-to-voltage conversion gain was observed to remain constant up to the highest fluences considered (10^{13}n/cm²). An increase of the leakage current by an order of magnitude was measured, which did not affect noticeably the pixel noise.The sensitivity of the chips to the neutron irradiation in terms of charge collection efficiency is displayed on Fig. 1 for both prototypes. The figure represents the charge collected by groups of 4 pixels in a cluster when the chips are exposed to a ^{55}Fe source. Charge losses are observed for fluences exceeding ~10^{12}n/cm² or few 10^{11}n/cm², depending on the prototype considered. The effect is likely to come from a reduction of the minority charge carrier's lifetime in the epitaxial layer. Other results, as well as a description of the test procedure, are available in [5].

The results obtained demonstrate that MAPS stand quite substantial neutron fluences, which makes them well suited for numerous applications. Their performance is of particular interest for their use in a vertex detector at a future e^+e^- linear collider, where fluencies well below 10^{11} n/cm² are expected. One should notice that the intrinsic performances of this new technology are still being explored. The observed limits in radiation tolerance should therefore not be considered as ultimate.

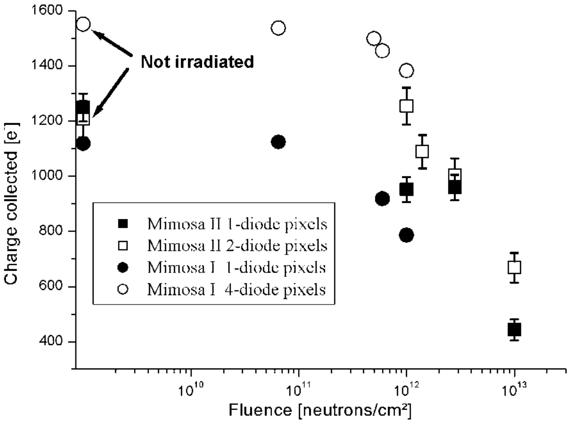

Fig. 1: Charge collected with MIMOSA I and II as a function of the neutron fluence. Error bars represent the spread of charge collection between different non irradiated MIMOSA II chips.

3. Full scale prototype

In order to apply the MAPS detector technology to a vertex detector in high-energy physics experiments, the performances achieved with the first small prototypes need to be reproduced with a large scale device (typically few cm^2). A first wafer scale MAPS prototype (MIMOSA V) has been designed and

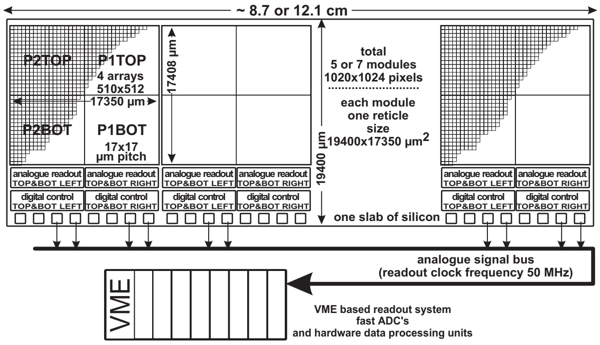

Fig.2 Schematic layout of a ladder equipped with MIMOSA V.

manufactured in a 0.6 μm CMOS process, in 2002. Its basic unit is a reticle size wide (19400 x 17350 μm^2) chip made of 10^6 pixels, grouped in four arrays of 510 x 512 active pixels. The pixels have a uniform pitch of 17 μm in both directions. Their architecture is close to the one of MIMOSA I. Each chip is equipped with four independent parallel analogue outputs. Because of the presence of long read-out lines exhibiting parasitic stray capacitance additional source followers placed at the end of each column has been added. The read-out chain and noise performance are optimized for the read-out frequency of 40 MHz. The read-out electronics was placed at the bottom of each unit, occupying a band of approximately 2 mm width (Fig.2).

The MIMOSA V prototype was tested with 120 GeV/c π^- at the CERN SPS in June 2002. The chip exhibited the detection efficiency close to 100% and a very high uniformity of the performance over the surface. The noise was about a factor 2 larger compare to the one of MIMOSA I. This was expected due to the additional source follower and the larger integration time. A S/N ratio of about 25 was observed. The spatial resolution was found to be ~1.7 μm which is slightly worse than with MIMOSA I because of larger noise. The total charge collected and its spread inside a cluster are similar to those of MIMOSA I (Fig.3) as expected from their identical fabrication processes.

The dependence of the chip performance on the incidence (θ) of the beam particles was studied. The total cluster charge follows to the expected $\cos^{-1}(\theta)$ function, and S/N in the seed pixel of the clusters grows up (Fig.4), reflecting the increase of the path length of the impinging particle in the active volume of the sensors.

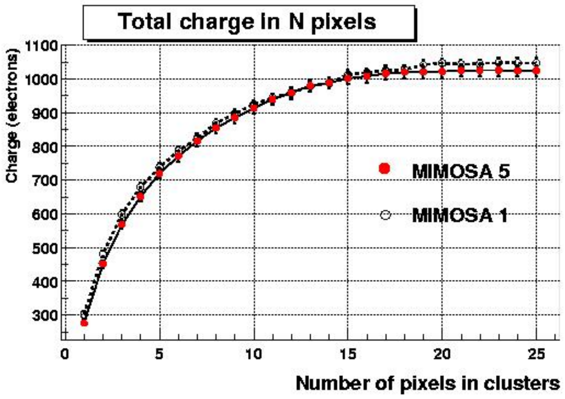

Fig.3 Collected charge (most probable value) as a function of the cluster multiplicity.

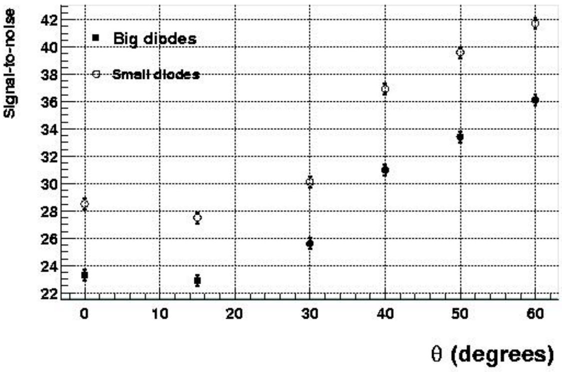

Fig.4 S/N in the seed pixel of MIMOSA V clusters as a function of the beam particle incidence for two different pixel design options.

4. First chip with integrated signal processing

The linear collider environment requires a typical integration or readout time of 50-100 μs. Taking into account the huge amount of pixels (up to 800 millions), it is desirable to design a chip architecture implementing on-chip signal processing with on-line data sparsification. A high readout speed will also require parallelism in the operations performed. The MIMOSA VI prototype was designed in this prospective. Recently fabricated in a 0.35 μm CMOS process, it can be considered as a first step aiming at implementation of signal processing functionalities, including data sparsification on-chip. The chip design features a single rectangular matrix of 30 x 128 pixels, with a pixel pitch of 28 μm. The pixel design includes on-pixel signal amplification with double sampling operation and provides a signal resulting from the difference between the charged collected in two consecutive frames. The pixel design uses only NMOS transistors, nwell/psub and pdiff/nwell diodes and poly1-to-poly2 capacitors. It is based on the principle of switched operation circuits with 15 transistors switches close to minimum size and 14 transistors used for the signal amplification. The chip readout is organized in a parallel way for 30 columns.

The detailed description of the design of MIMOSA VI can be found in [6]. First test results of the MIMOSA VI are expected by the end of the year.

5. Conclusion

Since 1999, five generations of CMOS MAPS for charged particle tracking have been designed and successfully tested. The excellent performances first demonstrated with small prototypes were reproduced recently with the full scale detectors. The measured hardness of the detectors to neutron irradiation exceeds the future linear e^+e^- collider requirements by more than two orders of magnitude. These results make the CMOS MAPS a good candidate for many applications where a precise high energy tracking is desirable.

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