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Monolithic Active Pixel Sensors (MAPS)

For Heavy Ion Experiments

Outline:

• CBM demands ⇔ Pixel detector performances

• Operating principle of MAPS

• Features of MAPS

• Development status report (thinning, radiation hardness, readout-speed)

Performances of different pixel-detectors

Comparing MAPS and established pixel-detectors

CBM demands (preliminary)fulfilled?	Hybrid pixels	CCDs	MAPS
Single point resolution	**No**	**Yes**	**Yes**
Material budget	**No**	**Yes**	**Yes**
Time resolution	**Yes**	**No**	**No**
Radiation hardness	**No**	**No**	**No**

What stands MAPS for?

Monolithic:

Readout-electronics and sensors are integrated on the same substrate.

Active Pixel :

Signal processing microcircuits are integrated in each pixel.

Sensor

MAPS were developed for visible light applications by industry.

MAPS may be produced with standard CMOS-processes.

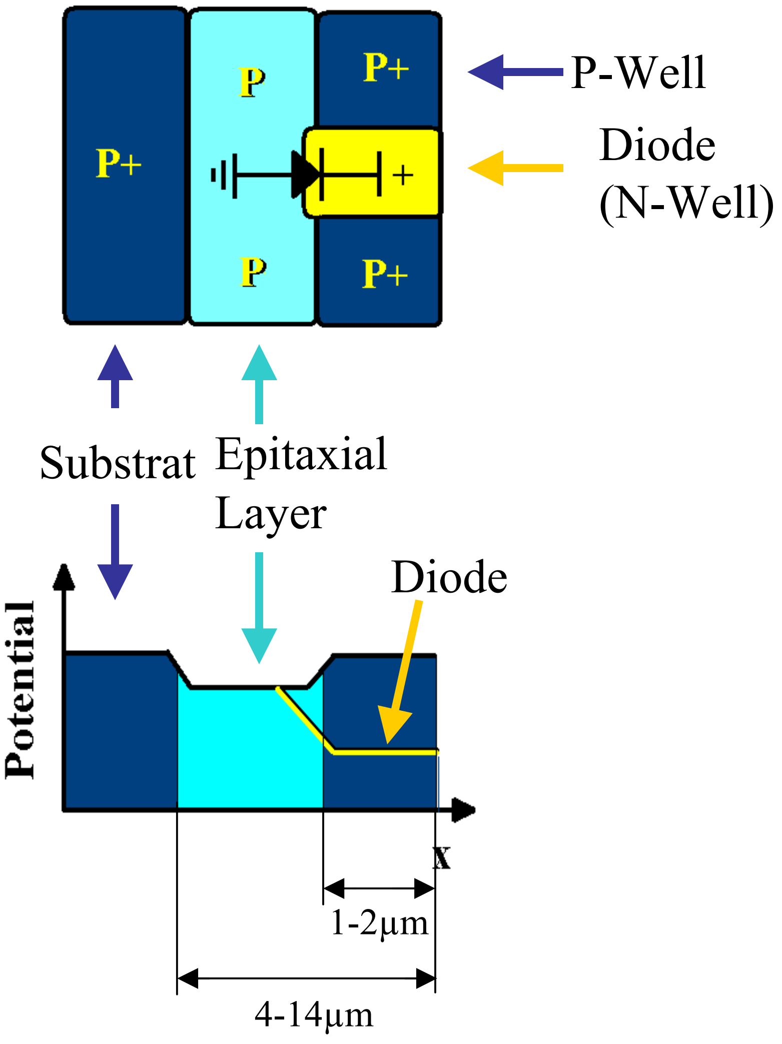
R&D for application on Futur Linear Collider since 1999 @ IReS

The operation principle of MAPS

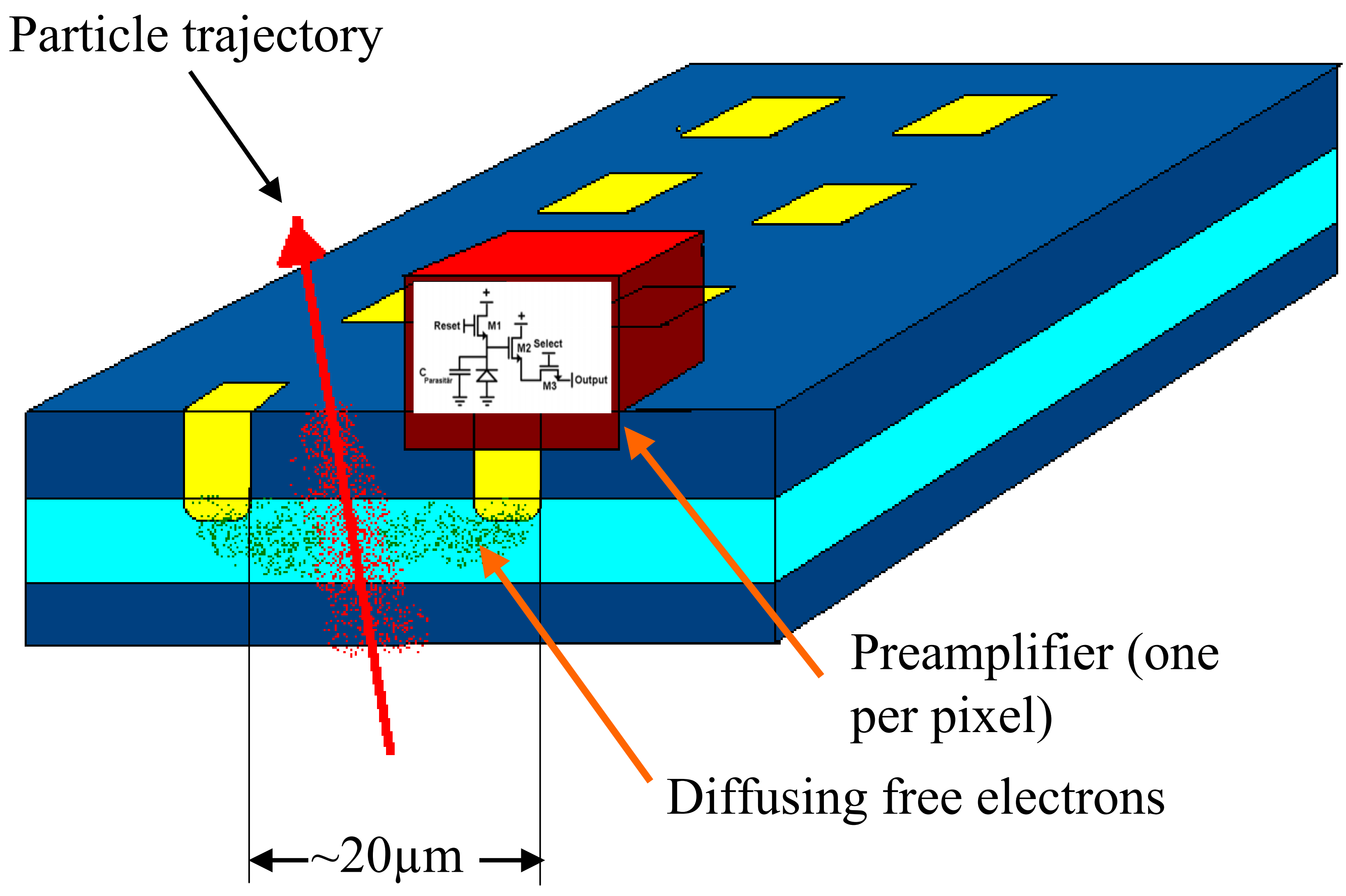
Sensor design:

A
Minimum
Ionising
Particle creates

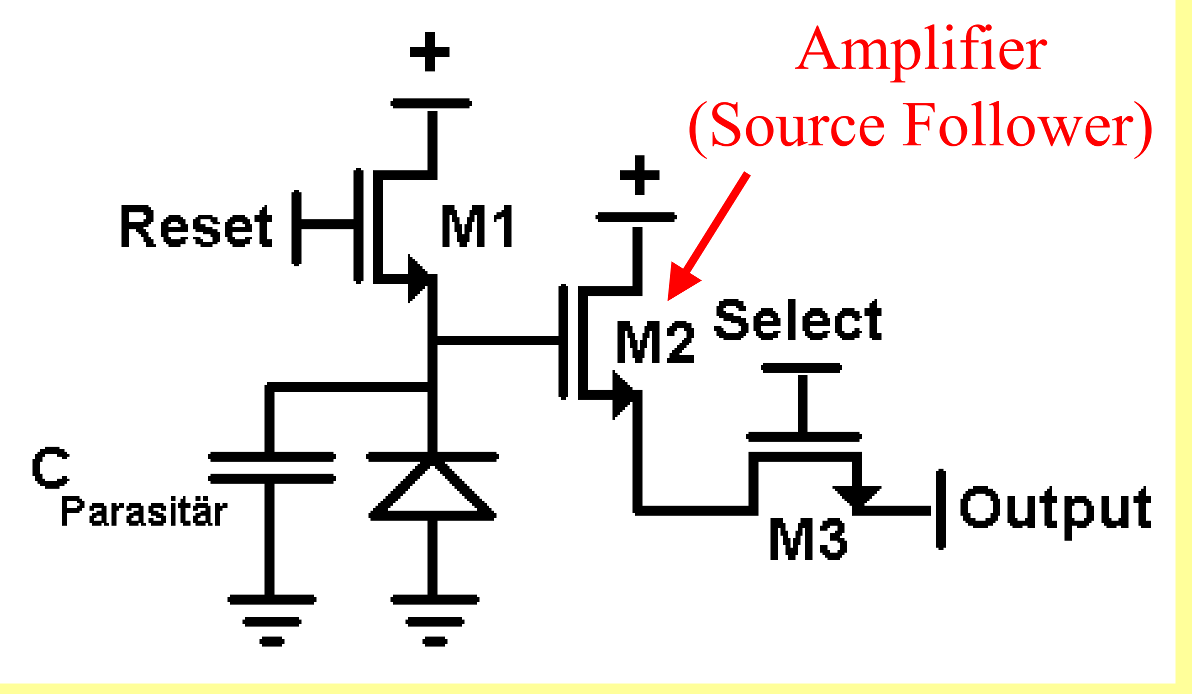
about 80 e^-/h-pairs per μm in Si



The operation principle of MAPS



The operation principle of MAPS

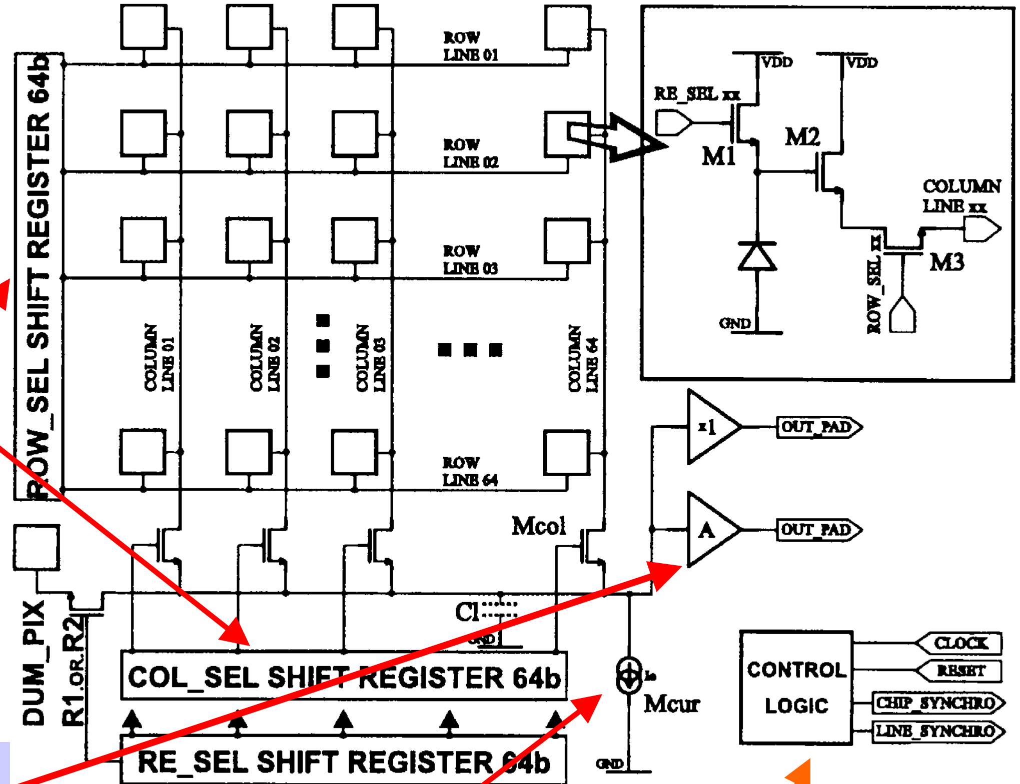


Layout of a classical Active Pixel (simplified)

The MIMOSA - technologie

Chip layout:

X- and Y-shift registers to select pixels.



Common amplifier

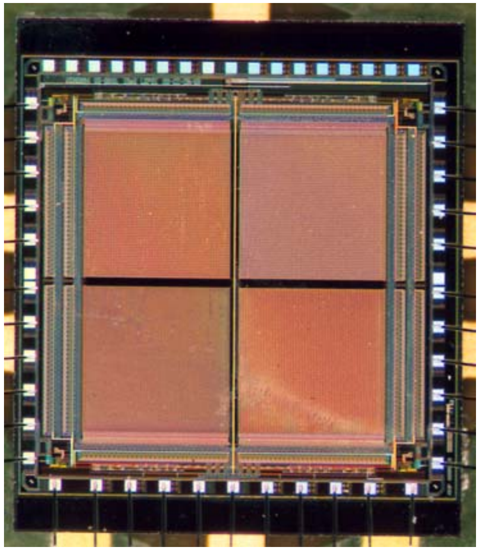
Current source

IO-Signals needed:

Clock, Reset, Synchro and analog out

The MIMOSA - Technology

Minimum Ionizing Particle MOS Active Pixel Sensor

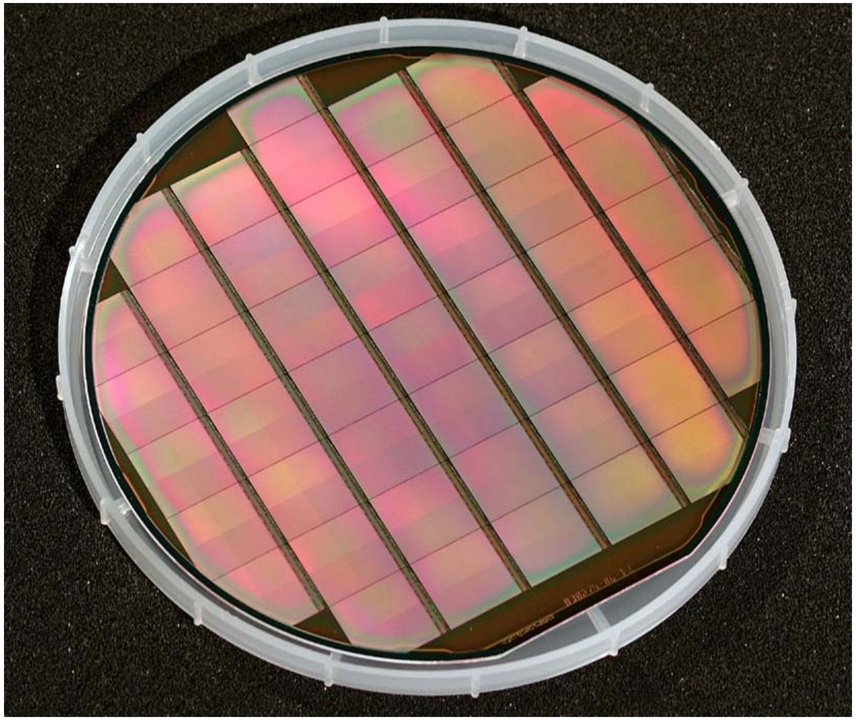


MIMOSA IV

Features of the MIMOSA (I – VI) – detectors:

- Single track resolution 1.3µm - 3µm
- Typical Pixel – pitch 20µm
- Thinning potentially possible down to ~20µm
- S/N for MIPs 20 – 40
- Readout speed: 10MPixel/s (design: 40MPix/s)
- Design tested on different commercially available CMOS-Processes
- 1k€ per 10^6 Pixel (Prototype)

Status and plans: Thinning



MIMOSA V Wafer

Goal:

$\lesssim$ 50µm/sensor

Present:

MIMOSA V (1MPixel / 3,5cm^2) thinned down to 120µm

Near futur:

Industrial thinning of MIMOSA V wafers to

~ (15µm Sensor + 25µm support).

Status and plans: Radiation hardness (ionizing)

Degradations occure after a few 100 kRad
(checked with β, X-rays)

Behavior observed after 200kRad X-rays:

MIMOSA II:

- **strong charge loss.**
- **Gain not degraded and constant.**

MIMOSA IV:

- **No charge loss.**
- **Gain slightly degraded and depending on temperature.**
- **Reasons for degradations mostly understood.**

Small changes in design improve the radiation hardness
=> more detailed understanding of design is necessary

Status and plans: Radiation hardness (ionizing)

Origin of weak points is under study:

•I -V and C -V measurements were done to learn about process parameters (doping profile...).

•Results are to be used as input for ISE-TCAD simulations.

•Test structures are implemented in current and future chips.

•First updated designs basing on preliminary understanding are implemented on new chips (Tests underway).

Status and plans: Radiation hardness (neutrons)

Charge losses occure for fluences higher than ~ 10^{12} n_{eq}/cm^2

Main problem:

Defect states in band gap (traps).

=> Decrease of charge carriers lifetime.

=> Decrease of charge collection and signal.

Standard approach (LHC):

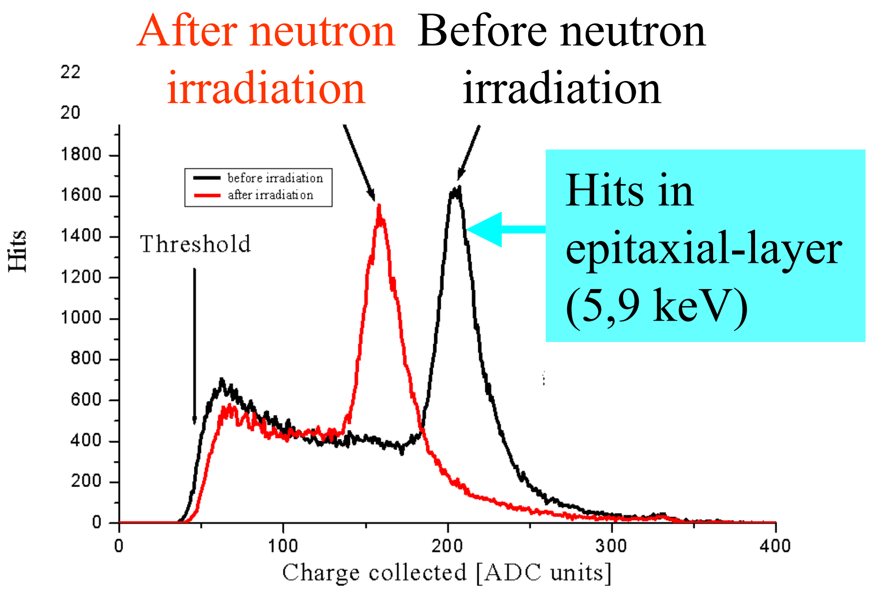
• Using depleted devices for fast charge collection.

Not compatible with industrial CMOS-processes.

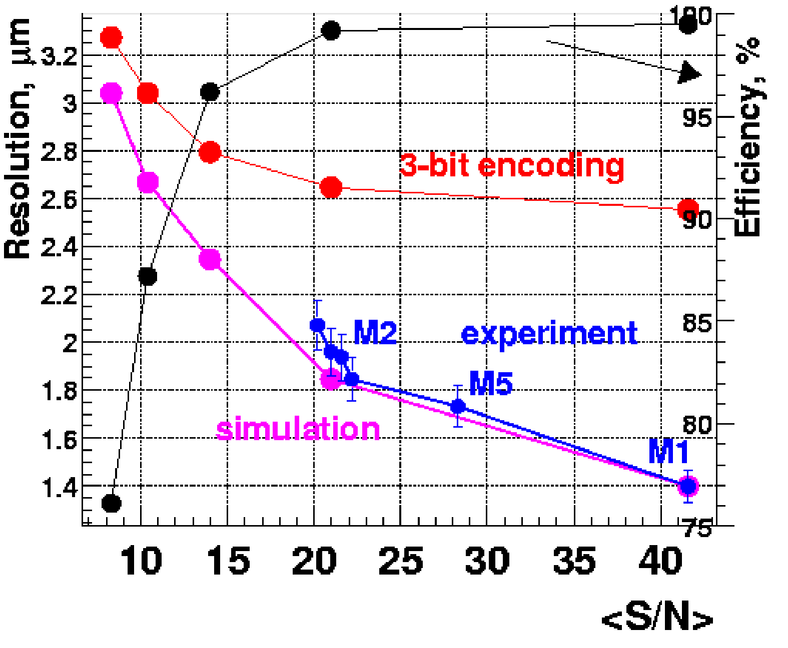
=> New ways are to be found

Status and plans: Radiation hardness (neutrons)

Charge collected



S/N versus resolution



- Pixels loose S/N => drop in detection efficiency.
- Readout electronics stays ok => Pixels die individually
- Resolution stays ok.

Status and plans: Radiation hardness (neutrons)

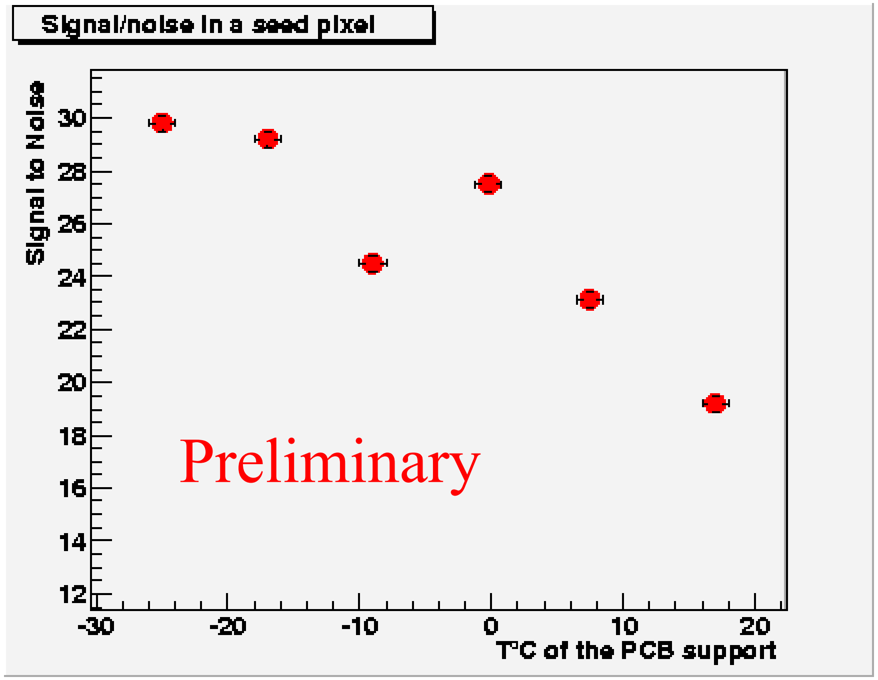
Approaches to be evaluated:

• Optimised pixel geometry (ISE -TCAD – Simulation)

• Temperature dependence of charge losses (Lazarus effect)

• Using sensors with better intrinsic S/N (PhotoFET)

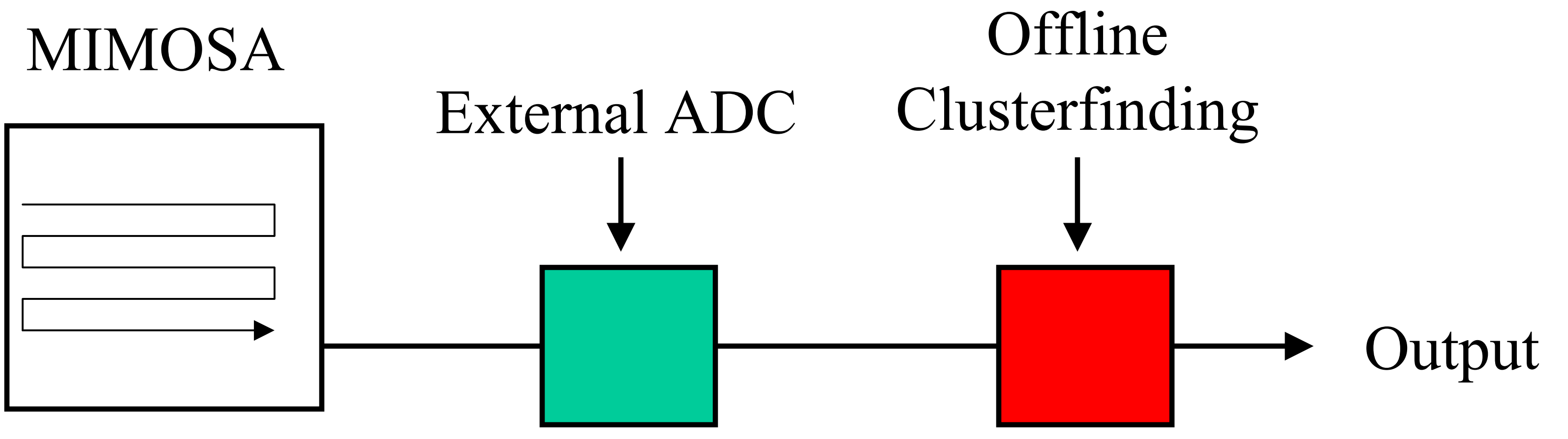
MIMOSA IV after 1.4 $10^{11} n_{eq}/cm^2$.
S/N in a seed pixel



Simple and relatively cheap approach to gain a factor 10-100:
Replacing the damaged area for example every month.

Status and plans: Readout speed

MIMOSA V needs ~ 6 ms for serial readout (1MPixel).



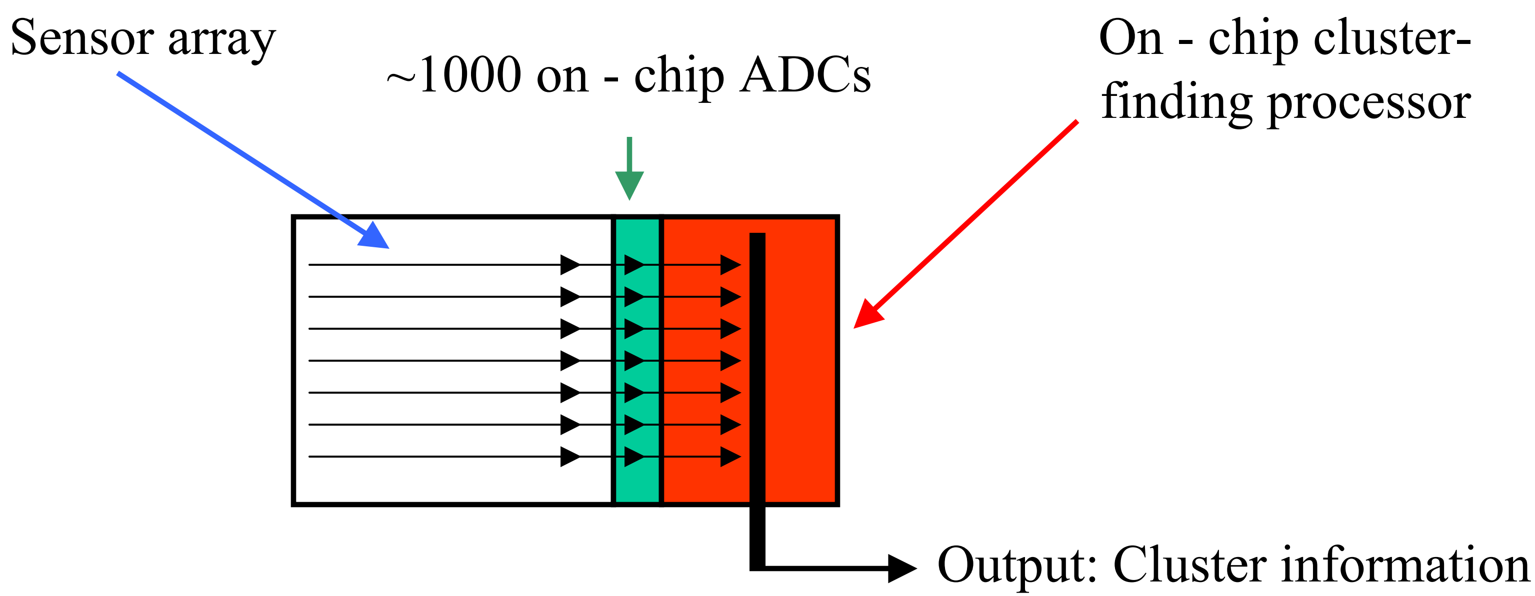
~40 Mpixel /s per analog output-line is possible

A factor 100 - 1000 may be won using a column parallel readout.

~100 GB / s dataflow for **1MPixel** is expected for 10µs/frame

Status and plans: Readout speed

Approach: On-chip real time data sparcification.



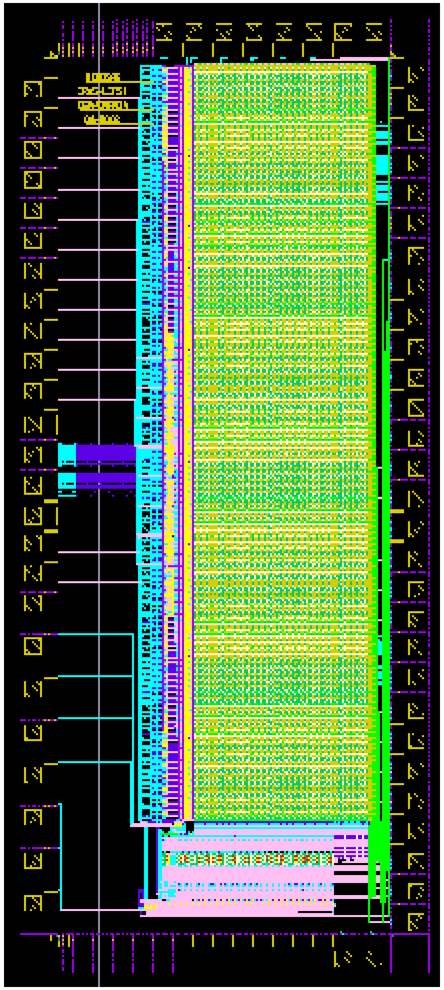
A CDS-Processor + memory must be included in each pixel

=> Individual pixel readout drops to ~10MHz

Goals: 250µs/frame in a first step, 10µs/frame within three years.

Status and plans: Readout speed

First prototype with column parallel readout: MIMOSA VI



<u>In every pixel (28µm pitch):</u>

- Additional amplification (5.5x)
- Analogue CDS processing
- 29 transistors, 3 capacitors

<u>In every column:</u>

- Discriminator

- **30 columns (128 Pixels each) with parallel readout**
- **30MHz clock, 5MHz readout (6 clocks per pixel)**

Tests under way

Summary

- **A single track resolution of 1.3µm - 3µm has been demonstrated for MAPS.**

- **Industrial thinning to ~ (15µm + 25µm) in near future**

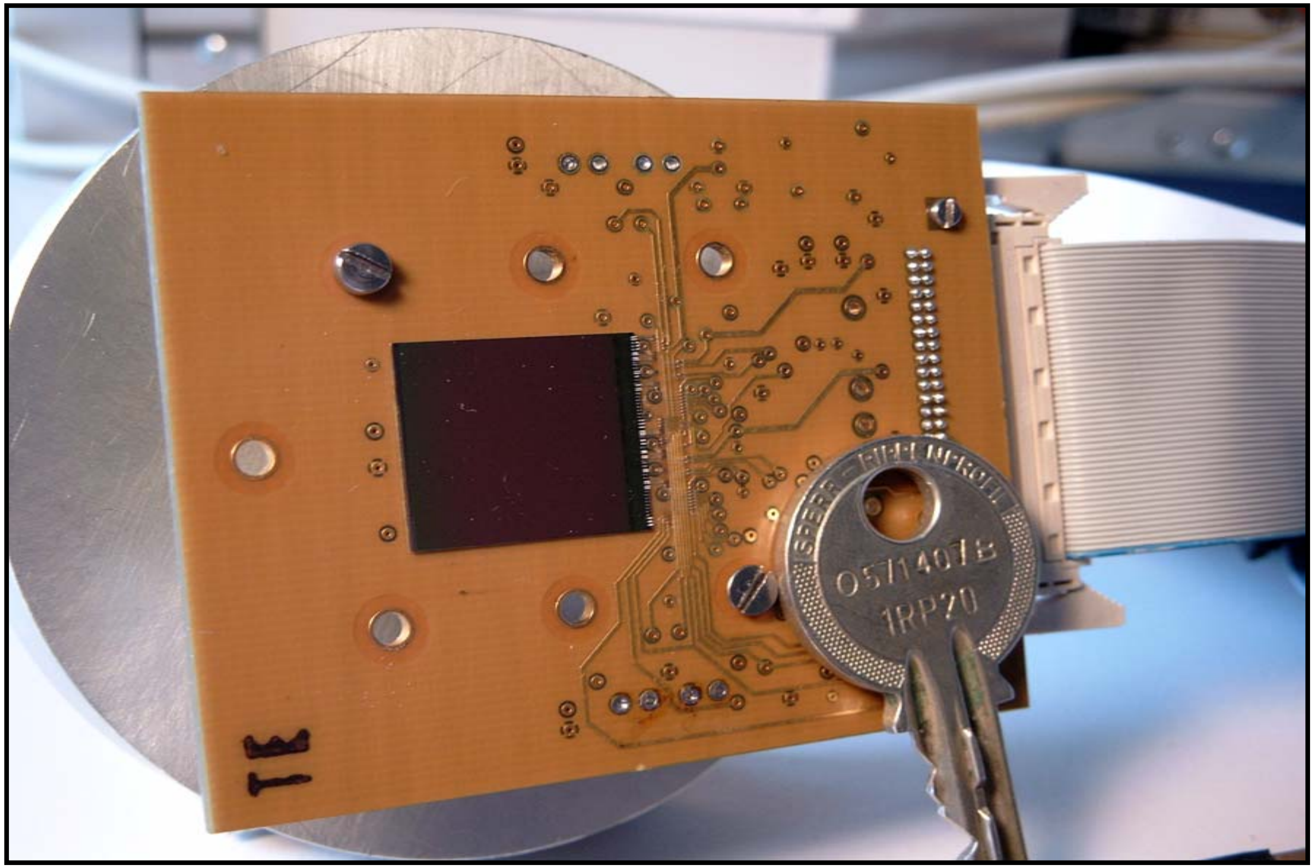
- **Column parallel readout should enable 10µs time-resolution in three years.**

<u>Intensive radiation hardness studies are underway</u>

- **detailed understanding of design for further improvement concerning ionising radiation**

- **evaluation of new approaches concerning neutron radiation (optimised geometry, low temperature…)**

Thank you



MIMOSA V

More information in the internet:
http://ireswww.in2p3.fr/ires/recherche/capteurs/index.html