

A Monolithic Active Pixel Sensor

for Charged Particle Tracking and Imaging

using Standard VLSI CMOS Technology



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ABSTRACT

A Monolithic Active Pixel Sensor (MAPS) for charged particle tracking based on novel detector structure has been designed, fabricated and tested. The device architecture is that of CMOS Camera, recently being proposed as an alternative to the standard CCD sensors in visible light imaging. The partially depleted thin epitaxial silicon layer is used as a sensitive detector volume. Semiconductor device simulation, using either ToSCA based or 3-D ISE-TCAD software packages shows efficient and reasonably fast (order of 100 ns) charge collection, with a charge spread limited to a few pixels only. Our first fabricated prototype contains four arrays of 64 by 64 elements each, with a readout pitch of 20 μm in both directions. Extensive tests made with soft X-ray source (^{55}Fe) and minimum ionising particles (15 GeV/c pions) fully demonstrate the predicted performances, with the individual pixel noise (ENC) at the level of 20 electrons and the Signal-to-Noise ratio for both 5.9 keV X-rays and Minimum Ionising Particles (MIP) of the order of 40. The device was fabricated using standard submicron 0.6 μm CMOS process, which features twin-well on a p-type epitaxial layer. These characteristics are common to number of modern CMOS large-scale submicron processes. This novel device opens new perspectives in high precision vertex detectors in Particle Physics experiments, as well as in other application, like low energy beta particle imaging, visible light single photon imaging (using Hybrid Photon Detector approach) and high precision slow neutron imaging.

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I. INTRODUCTION

In the early 90's monolithic pixel sensors have been proposed as a viable alternative to CCD's in visible imaging [1]. These sensors are made in a standard VLSI technology, usually CMOS, which is the reason why they are usually called CMOS imagers. Today's CMOS imagers most popular basic cell architecture (Fig.1) consists of photosite (photodiode or photogate) integrated together on an individual pixel with three transistors: a reset switch, the input of a source follower and a selection switch. Such architecture allows electron noise of less than 10 electrons r.m.s. at room temperature.

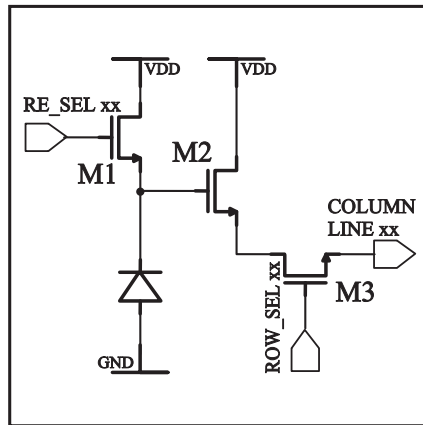


Figure 1. The baseline architecture of CMOS imager. Transistor M1 resets the photosite to reverse bias, transistor M3 is a row switch, while transistor M2 is the input of a source follower. Follower's current source (common to entire row) and column selection switch are located outside the pixel.

CMOS sensors feature several advantages with respect to the more generally used CCD's: they are fabricated in a fully standard VLSI technology, which means low costs; taking advantage of submicron CMOS technology, may be radiation hard; several functionalities can be integrated on the sensor substrate, including random access; they consume very little power as the circuitry in each pixel is active only during the readout and there is no clock signal driving large capacitance. Because of these characteristics, CMOS sensors are the favoured technology for demanding application, which are typically found in space science.

In visible light application, special care is taken to maximise the fill factor, i.e. the fraction of the pixel area that is sensitive to the light. Because of the transistors, fill factors in CMOS sensors are relatively low (in the order of 30%). This can be a severe limitation in particle tracking application, if no special care is taken. One of us [2] proposed to integrate a sensor in a twin-well technology with an n-well/p-substrate diode in order to achieve 100% fill factor for ionising particle detection (Fig.2). This technique has already proven its effectiveness in visible light application [3] reducing the blind area to the routing metal lines, clearly opaque for visible light but not affecting the charge particle detection.

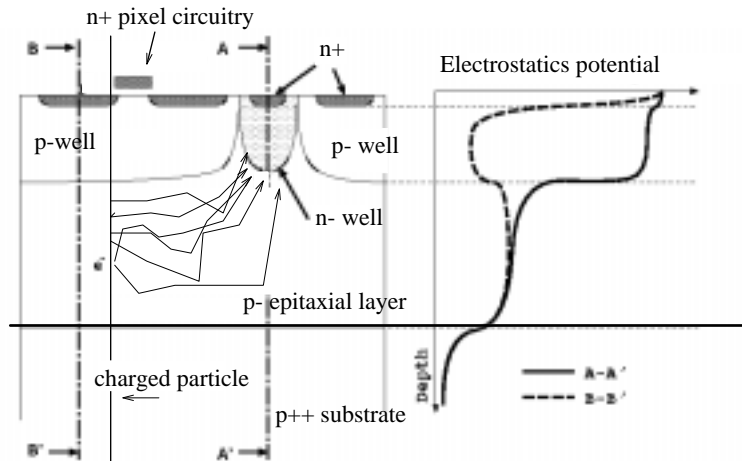


Figure 2. Internal structure of a pixel for charged particle tracking. The circuit's three transistors are integrated in the p-well while the charge-collecting element is an n-well diode on the p-epitaxial layer. Because of the difference in doping level (three orders of magnitude), the p-well and the p++ substrate act as reflective barriers. The generated electrons are collected in the n-well [3].

CMOS sensors could achieve high spatial resolution: the pixel size is usually between 10 and 20 times the Minimal Size Feature of the used technology, which means that 10 μm 2-D pitch is possible, and hence spatial resolution better than 3 μm even with a binary readout. Taking advantage of possible analog readout and natural charge spread between neighbouring pixels, for very demanding application the spatial resolution can possibly be pushed down to less than 1 μm . At the same time, very low multiple scattering is introduced as the substrate can in principle be thinned down to a few tens of microns. A charge particle CMOS detector would also benefit from the generic characteristics of these devices, including low power dissipation, radiation resistance of deep submicron CMOS technologies and low cost.

To provide a prove-of-principle of CMOS sensor application for the detection of charged, minimum ionising particles, we have designed, fabricated and tested a prototype chip (MIMOSA = Minimum Ionising particle MOS Active pixel sensor) using standard 0.6- μm CMOS technology by AMS. In this work we present design consideration, semiconductor device simulation, calibration using soft X-ray source and first results with high energy, minimum ionising particles. A more detailed analysis of the beam test data is currently under way and will be presented elsewhere.

II. DEVICE SIMULATION

Detector principle

In a CMOS sensor, the detector part is made of low resistivity silicon. The depletion region is shallow and consequently charge collection efficiency poor. The proposed pixel structure can overcome this limitation by extending the active volume to the partially depleted p-type epitaxial silicon, grown on a highly doped p⁺⁺ substrate. Incident radiation produces excess carriers in the epitaxial layer [fig.2] and the electrons diffuse towards the n-well diode contact within a typical time of a few tens of nanoseconds. Because of the three orders of magnitude difference in doping levels between the p-epi-layer and the p⁺⁺ wells and substrate, potential barriers are created at these boundaries, which acts like mirrors for the excess electrons (minority charge carrier). Inherently, substrate is formed of "low quality" silicon and the recombination time in this region is relatively short. As a matter of fact p⁺⁺ substrate behaves as a getter for the impurities. Relatively short recombination time in the substrate is a reason for which only a small part of the charge created there is supposed to be able to drift towards the epitaxial layer and then to be seen by collecting electrodes.

Tracking in Particle Physics experiments requires detection of minimum ionising particles (MIPs). This means detection of each single particle with high efficiency and good spatial localisation. A relativistic charged particle releases only a fraction of its energy in a thin layer of matter: it generates typically 80 pairs of electron-holes per micron of silicon. In addition, the charge is usually shared between two or more pixels. Commercial CMOS sensors (with epitaxy thickness of 3-5 μm) are not optimised for this application. The process for the MIMOSA chip has been chosen bearing in mind on commercially available technology that offer wafers with

thick epitaxial layer. Finally the AMS CUP process characterised by epitaxial layer thickness between 12-16 μm , providing a MIP signal of about 1200 e^-/h^+ , was used. The diode collecting volume is formed by the pattern of 3×3 μm N-well structure, that paves the way for the epitaxial layer forming the potential well that collects the charge. In addition, one quarter of MIMOSA has a new four-diode structure that is supposed to limit the charge spreading to very few neighbouring pixels. Two series of simulation studies have been made, in order to validate the "thick epitaxy" choice. If a larger epitaxial layer provides obviously more charge per MIP, we expect also more than one pixel being involved in each event (charge sharing) as well as a longer collection time (competition with recombination). Besides the collected charge in the central pixel (Q_c), which is of paramount importance for cluster search, we defined three other output variables: the charge spreading between adjacent pixels (σ_Q), the average signal in the cluster (Q_{clu}), and the collection time (t_{coll}) in each pixel of a cluster. A 3×3 -pixel subarray around the pixel showing the largest signal defines a cluster. For a given pixel size, we have identified four physical parameters that have the most decisive effect on the above defined variables: the thickness d_{EZ} of the epitaxial layer, the width d_{EZP} of the boundary region between the epitaxy and the p^{++} substrate (which act as a smooth gradient of potential), the depth d_N of the N-well collecting diode and the electron recombination time τ_R .

Monte-Carlo study

The optimal configuration was studied first by Monte-Carlo, as the physical process is transport at thermal velocity, together with diffusion, and an additional electric field in a few regions (boundaries of the epitaxial layer, collection diode). The field profiles are deduced from two-dimensional device simulations made with ToSCA [4]. The recombination time of the minority carriers was considered as a totally unknown parameter. Device parameters like d_{EZ} and d_N are given by the manufacturer with quite large error bars: these two essential device parameters are thought to be in the range of 12 to 15 μm and 2 to 4 μm respectively. For the epitaxy-substrate interface, the fact that the wafer is processed at high temperature implies that in the simulation one needs to consider also a several microns wide transition zone: we can suppose $2 \mu\text{m} < d_{EZP} < 5 \mu\text{m}$. Hereafter the quantitative simulation results for a "central" hit (centre of the pixel), compared to a track hitting one corner of the pixel (Fig.3). The full details of these studies may be found elsewhere [5].

Table 1 gives the Monte-Carlo simulation results for the single-diode geometry. We compare the most favourable case and the worst one, depending on track position inside the pixel: these calculations show that the MIMOSA will provide a high charge signal for single MIPs for all kind of tracks. Most difficult to detect are the tracks hitting the corner of a pixel, who must share the released charge between four neighbouring pixels, but this study shows that the charge in the central pixel of the cluster is always high enough to allow efficient cluster selection, supposing electronics noise at the level of few tens of electrons.

	'central' hit			'on corner' hit		
d_{EZ}	9 μm	12 μm	15 μm	9 μm	12 μm	15 μm
Q_c [electrons]	740	750	760	160	165	170
Q_{clu} [electrons]	900	1000	1100	720	800	850
σ_Q [pix]	0.30	0.40	0.51	0.73	0.87	0.92
t_{coll} [ns]	5.1	10.2	14.5	17.3	23.0	26.4

Table 1. Collection efficiency parameters for a single MIP particle.

The N-well diode depth and the electron recombination time may have important effects on charge collection. In Table 2, we summarise the sensitivity of charge collection to these two parameters. Our calculation shows that the recombination time would limit the collection efficiency only for very low value of τ_R , but in high quality epitaxial silicon, we expect that recombination will have a limited impact on charge collection efficiency. The conclusion of this study is that a minimum ionising particle provides a cluster total signal of about 900 electrons, for any reasonable assumption concerning process parameters value.

	d_N as a variable			τ_R as a variable		
	2 μm	3 μm	4 μm	150 ns	300 ns	600 ns
Q_c [electrons]	660	750	830	670	680	700
Q_{clu} [electrons]	1000	1100	1160	990	1010	1040
σ_Q [pix]	0.53	0.51	0.44	0.19	0.40	0.45
t_{coll} [ns]	18.7	14.5	12.3	13.3	15.1	17.2

Table 2. Effects of device parameters on collected charge for a central hit.

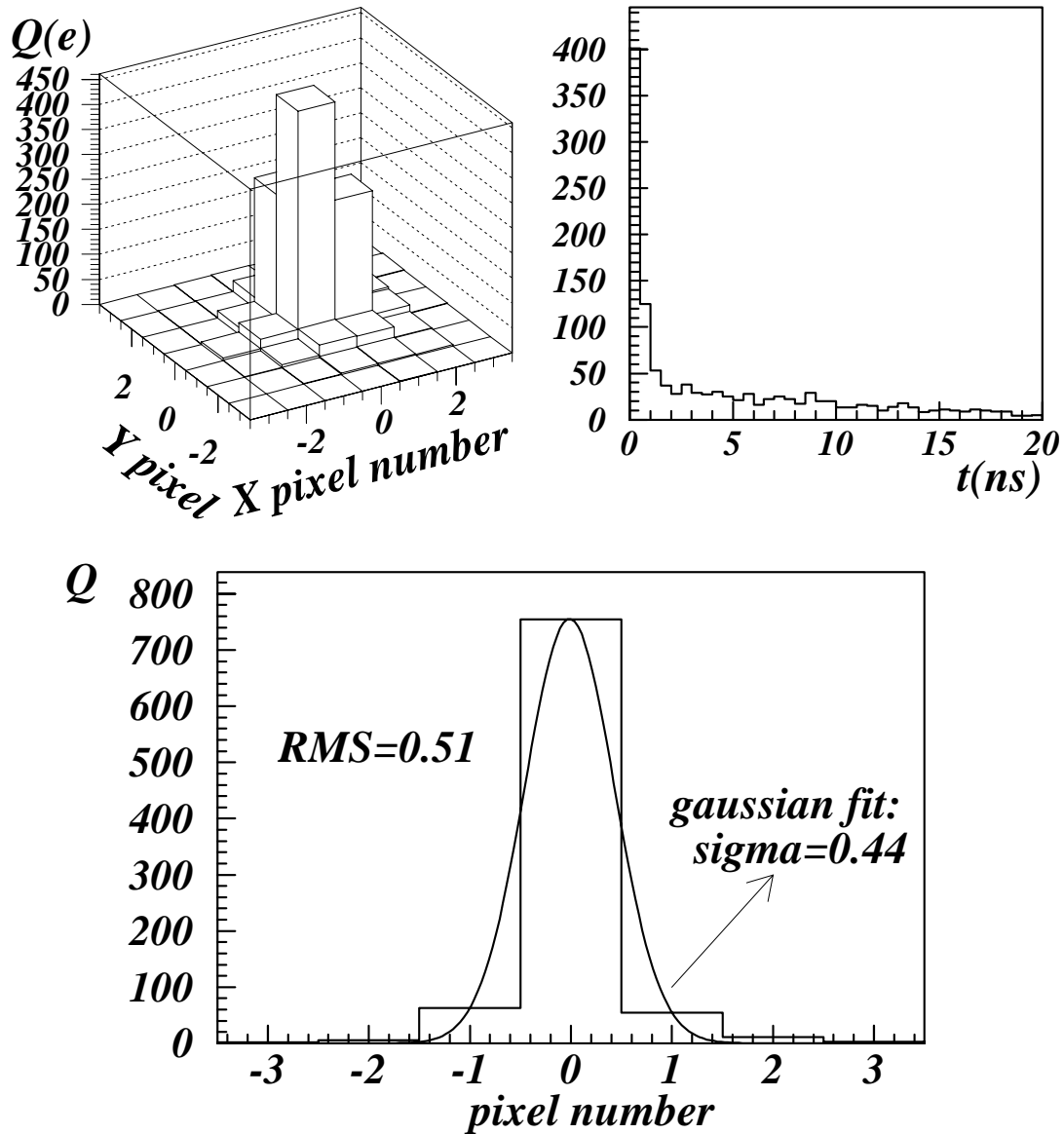


Figure 3. Monte-Carlo results: 3-D charge spreading and collection time distribution for a 'typical' hit (above) and a 2-D projection of the cluster in the case of 'central' hit (below).

Full 3-D simulation

The usefulness of 2D simulations for pixel detectors, which are actually 3D devices, is limited. Also, so as to succeed with optimisation of pixel architecture, taking into account all possible physical and technological parameters, some advanced tool allowing for technological process and 3D device modelling is essential. Therefore commercially available ISE-TCAD [6] package was used. Simulated structure is described by the boundary inside which the mesh and doping profiles are defined. The granularity of the mesh is adjusted to the

gradient of the impurity concentration and to the demanded calculation precision in some critical parts of the detector volume. Thanks to the AMS (Austria Mikro Systeme International AG) it was possible to carry out 3D simulation using doping profiles definition that are very close to the real AMS 0.6 μm process in which our detector was fabricated. In spite of theoretically unlimited number of grid points on which ISE-TCAD can work, the number of mesh vertices used in simulation was limited to the reasonable value of 50000-60000. This upper limit results from limited capacity and calculation speed of the computer (HP9000/778). The most important benefits, coming from the use of the ISE-TCAD package, are advanced physical models that are implemented in the package. The appropriate physical models for effective intrinsic density, carrier mobility, recombination, impact ionisation have been chosen for simulation and their parameters were calculated either on the basis of impurity concentration or given explicitly taking into account standard parameters of silicon. The drift-diffusion model has been chosen for solving the problem of charge collection. The structures of 3x3 pixels were simulated. Due to the reflective (Neumann) boundary conditions, an additional volume of silicon was added on every side of the core cluster. Thickness of the detector used in the simulation was limited to 25 μm included 15 μm of the epitaxial layer, which is a typical value in the AMS CUP process. We take into account only 10 μm of the substrate (to speed up simulation time) because in first approximation the substrate was assumed to be of no importance for the useful signal. The latest is probably not true, but in order to incorporate real substrate layer into the simulation it is necessary to know more details about the properties of the substrate (trap densities, recombination time etc.). The alpha-particle model with gaussian dependence on radial co-ordinates was chosen for charge generation. Simulations are carried out with a charge of 80eh/ μm created along the trace of the particle. Simulation methodology applied in ISE-TCAD is different from the Monte-Carlo approach presented before. Instead of tracing separately each carrier, the collected charge is obtained by current integration. Both simulation methods give comparable results, which are in good agreement with measurements. Further improvement in simulation precision and better understanding of the charge collection in the MAPS needs much more accurate technological information. Actual MIMOSA simulation results for MIPs using ISE-TCAD package are presented in fig 5, 6 and 7. Geometry used in simulation is shown in fig.4.

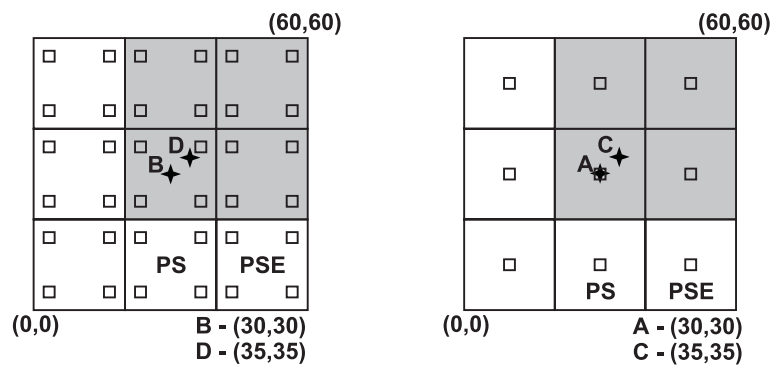


Figure 4. Particle impact position for 4-diode and single-diode type 3x3 pixel arrays. Terminology used further in simulation results is highlighted in this figure.

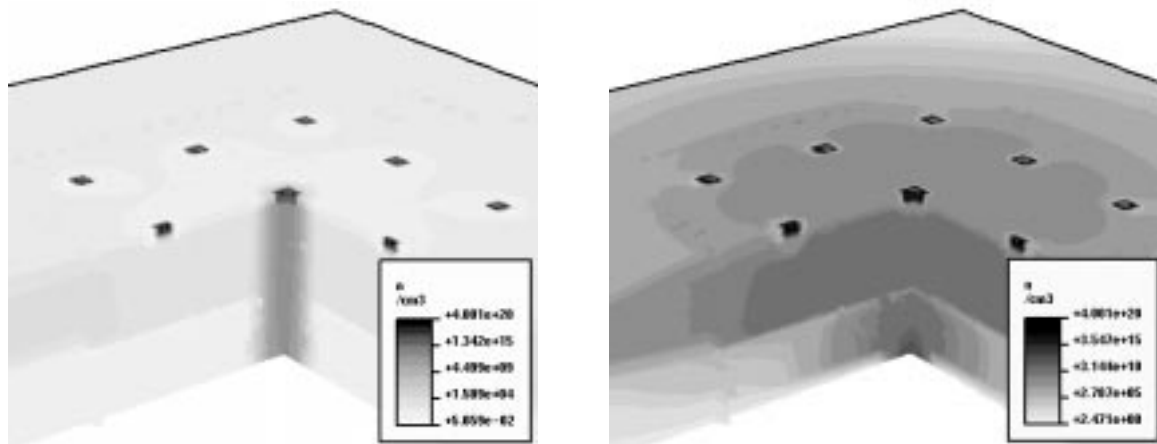


Figure 5. Carrier concentration at 1 MIP charge injection time (left) and 25ns later (right). Charge was injected in the centre of 1-diode type pixel (fig.4, case A). A cluster of 3x3 pixels was simulated. Simulated layer is 25 μm thick including 15 μm of epitaxial layer.

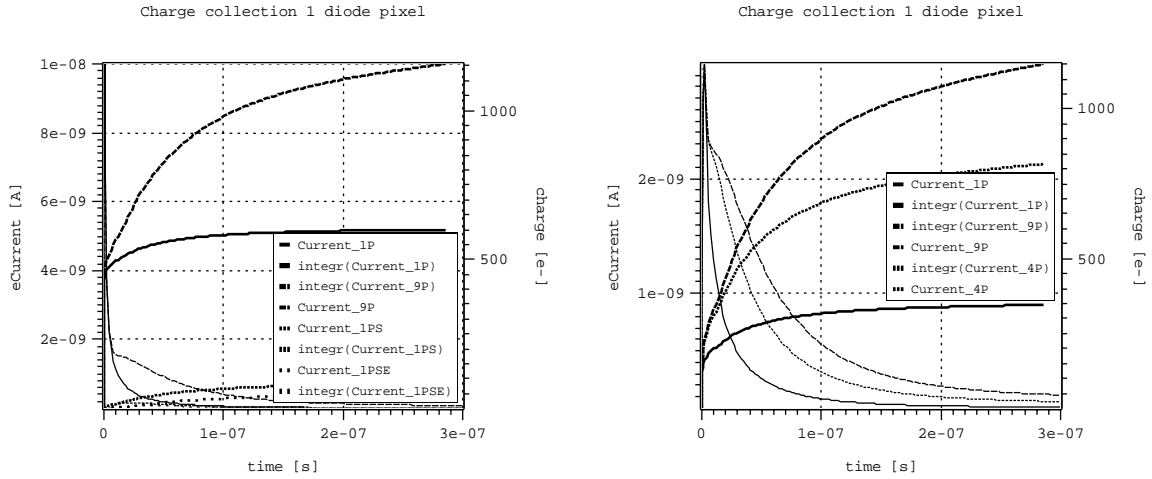


Figure 6. Charge collection in the cluster of **single-diode type** pixel array in case of central (left) and side hit (fig.4, A and C). Apart of result for the central pixel (1P) and the cluster (9P), data for closest neighbour (PS), for closest corner neighbour (PSE) and 4 pixels closest to the impact position (fig 4, grey area) are also presented.

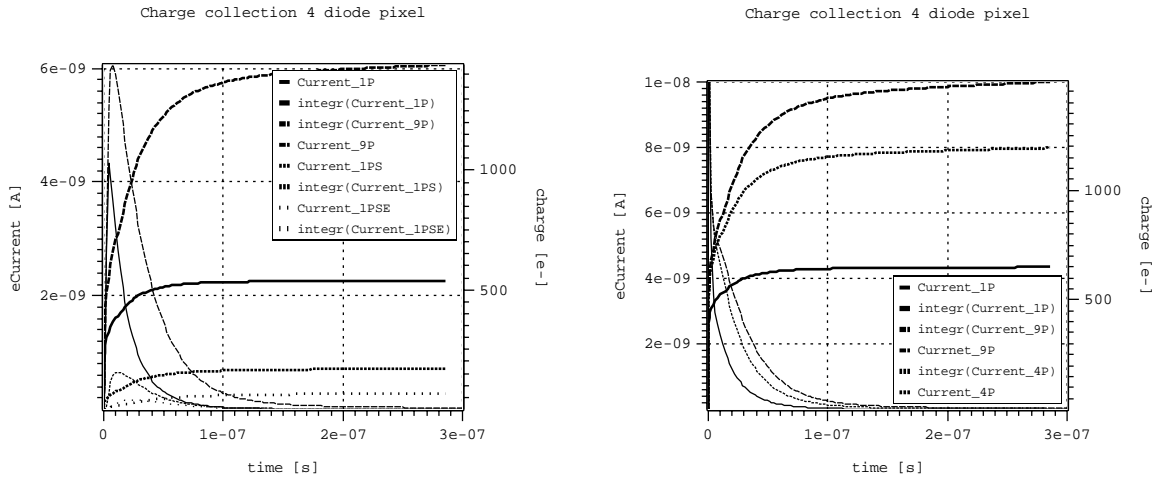


Figure 7. Charge collection in the cluster of **4-diode type** pixel array in case of central (left) and side hit (fig.4, B and D). Apart of result for the central pixel (1P) and the cluster (9P), data for closest neighbour (PS), for closest corner neighbour (PSE) and 4 pixels closest to the impact position (fig 4, grey area) are also presented.

III. PROTOTYPE DESIGN

Main features

The prototype chip consists of 4 independent arrays of active pixels having slightly different design [7]. Each array is made up of 4096 pixels laid down in 64 rows and 64 columns with a pitch of $20\mu\text{m}$ in both directions. The first and basic idea is to use pixel architecture with only one n-well/p-epi diode (right), which is an optimum solution for the noise and conversion gain. The second approach is a four-diode architecture that is supposed to limit charge spreading between neighbouring pixels (left). However the negative side of the latter solution is substantially higher sensitive node capacity, with its direct effect on noise (increase) and conversion gain (decrease).

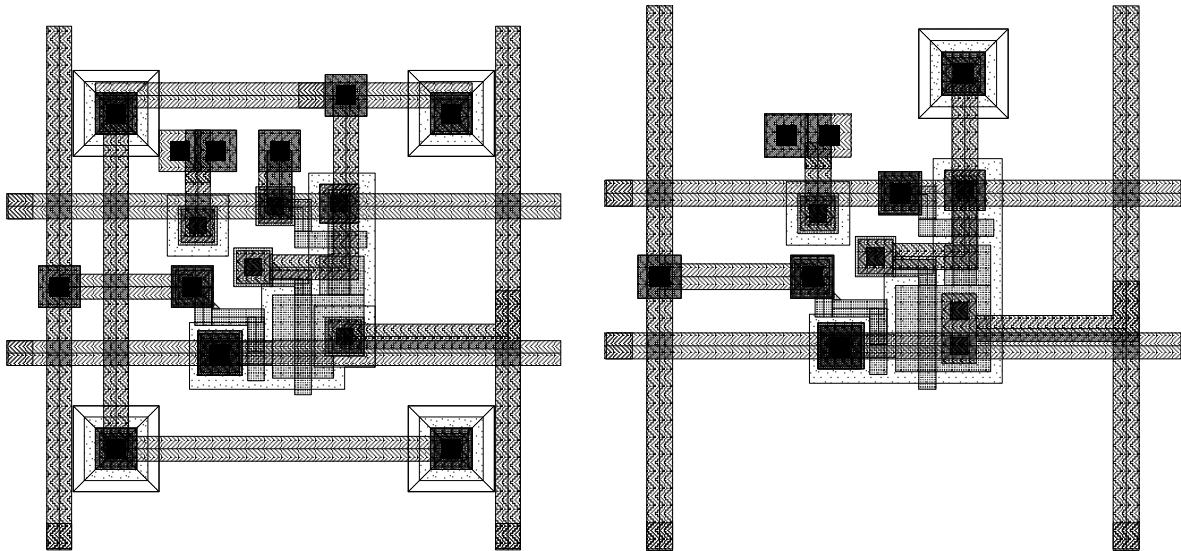


Figure 8. Example of basic cell layout: four-diode pixel (left) and single-diode pixel (right). Metal 3 layer not shown.

In addition to the block of pixels, each array contains three 64-bits long shift registers, an output source follower, an output voltage amplifier and one dummy pixel with its control system (fig.9). Because of relatively small array dimensions, a simple architecture with only one current source for entire array was chosen. Only CLOCK and RESET signals are necessary for the readout. The readout starts with single pulse on the RESET line and in 64 clock cycles the whole chip is reset. In every clock cycle, RE_SEL signal for one column of pixels is activated and all pixels in that column are reset. Then individual pixels are addressed in consecutive clock cycles. Operation of reset must be repeated every several/dozens frames. Minimum frequency of reset depends on the value of the diode leakage current that increases with temperature. Two analog outputs are available on a chip: direct output of the source follower and an amplified one providing a voltage gain of 5. This approach was expected to limit possible outside interference on the output signal. The dummy pixel, shown in the block diagram, is connected to the output line during the reset phase. This limits the output recovery time after a reset cycle. Positive analog power supply, bias and analog outputs are separate for each array. Digital power supply and both analog and digital grounds are common. The entire array of active pixels as well as the analog part of readout electronics is surrounded with a double guard-ring in order to prevent interference between different parts of the chip. The third metal layer is used to shield readout electronics and transistors in the pixel against visible light. Some area of the pixel is not covered by the shield, allowing test with visible light.

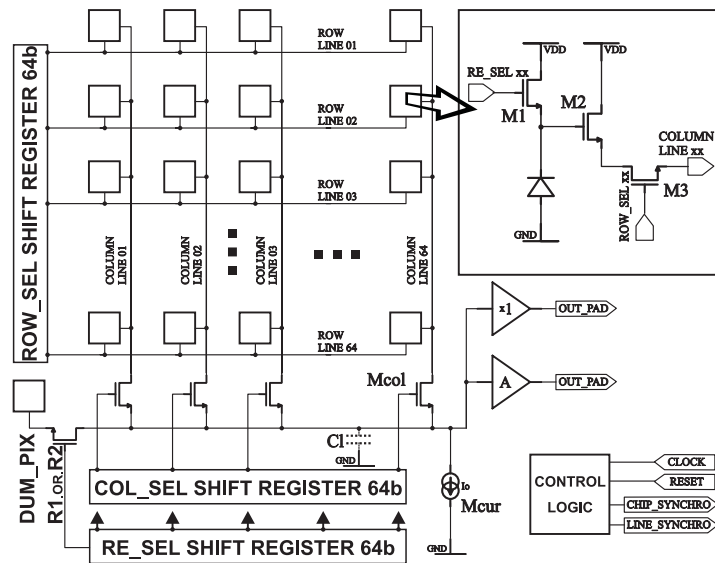


Figure 9. The simplified block diagram of a single array.

Noise consideration

Temporal noise sets a fundamental limit on active pixel sensors performance. This constraint becomes much more significant in particle tracking applications with respect to high luminosity video imaging. The main sources that contribute to temporal noise are due to the pixel reset (kTC noise), voltage follower and line/row access transistors. At first approach noise generated in the output voltage amplifier as well as in off-chip circuits can easily be neglected. The full analysis of noise is moreover complicated, mainly due to the nonlinearity of the charge to voltage conversion realised on a pixel, and to the reset transistor switching over. The reset transistor operates below threshold during most of the reset time and thus weak inversion must be considered. The noise analysis must be done separately for all three states of sensor operation i.e. reset, integration and readout [8].

Noise during reset

During reset, transistor M3 (fig. 1) is turned off and a positive voltage pulse is applied to the gate of M1. The M1 is saturated during a short time and then it goes below threshold for the rest of the reset time. If the reset time t_r is much greater than the settling time t_{settle} , it can be said that steady state has been achieved. Time t_{settle} represents the moment at which the reset transistor subthreshold current equals the value of the diode leakage current. The average reset noise power can be calculated in this case by means of the commonly known expression:

$$\overline{V_{n,res}^2} = \frac{kT}{C_d}$$

Here, C_d represents the total node capacitance that is found at the input of the source follower. However, in real systems reset time is not long enough to allow achieving steady state. In this case, the new value of average reset noise power is calculated by:

$$\overline{V_{n,res}^2} = \frac{1}{2} \frac{kT}{C_d}$$

Depending on the reset frequency one of the above expressions should be chosen for the reset noise evaluation.

It must be pointed out that the reset noise as well as so called Fixed Pattern Non-uniformity (FPN) can be removed using Correlated Double Sampling (CDS) technique. In our case CDS was done off-line by software during data analysis.

Noise during integration

The dominant noise source during the integration phase is shot noise due to the diode leakage current i_{leak} . At room temperature the mean value of this current is in the order of several fA, and the related noise contribution is not significant. However, this type of noise should be taken into account when time of integration is relatively long. For more precise noise analysis one should also take into account the diode capacitance change during the integration time. The capacitance change effect is a second order effect and is neglected in this noise calculation. Finally, the mean square value of the noise sampled at the end of integration (t_{int}) is given by:

$$\overline{V_{n,int}^2(t_{int})} = \frac{q i_{leak}}{C_d^2} t_{int}$$

Noise during readout

During readout, the transistors M2, M3 as well as the column switch M_{col} and the source follower current source M_{cur} with line capacitance C_l (fig. 1, 9) are the main noise sources. At first approach, the influence of $1/f$ noise can be neglected and only thermal noise contributions may be taken into account. Noise contributions introduced by each transistor can be calculated according to the expressions given below:

$$\overline{V_{n,read,M2}^2} = \frac{2}{3} \frac{kT}{C_l} \frac{1}{1 + \frac{g_{m,M2}}{g_{ds,M3} + g_{ds,Mcol}}}$$

$$\overline{V_{n,read,M3}^2} = \frac{kT}{C_l} \frac{1}{g_{ds,M3} \left(\frac{1}{g_{ds,M3}} + \frac{1}{g_{ds,Mcol}} + \frac{1}{g_{m,M2}} \right)}$$

$$\overline{V_{n,read,Mcol}^2} = \frac{kT}{C_l} \frac{1}{g_{ds,Mcol} \left(\frac{1}{g_{ds,Mcol}} + \frac{1}{g_{ds,M3}} + \frac{1}{g_{m,M2}} \right)}$$

$$\overline{V_{n,read,Mcur}^2} = \frac{2}{3} \frac{kT}{C_1} g_{m,Mcur} \left(\frac{1}{g_{ds,M3}} + \frac{1}{g_{ds,Mcol}} + \frac{1}{g_{m,M2}} \right)$$

Total noise

Total noise $\overline{V_n^2}$ at the output stage of the pixel is given the quadratic sum of all previously calculated noise components:

$$\overline{V_n^2} = \overline{V_{n,res}^2} + \overline{V_{n,electron}^2}$$

$$\text{Where } \overline{V_{n,electron}^2} = \overline{V_{n,int}^2} + \overline{V_{n,read,M2}^2} + \overline{V_{n,read,M3}^2} + \overline{V_{n,Mcol}^2} + \overline{V_{n,read,Mcur}^2}$$

The last expression represents contribution to the total noise that is not suppressed by CDS.

Main parameters and estimated performance of the MIMOSA prototype.

Simulations results were obtained for $T=27^\circ\text{C}$ and $V_{DD}=5\text{V}$ with reset transistor dimensions $W/L=0.8/0.6$. Noise is calculated for a line capacitance C_1 of 300fF and integration noise is not included. Table 3 resumes basic parameters and estimated performance of MIMOSA prototype.

supply voltage	single 4÷5V	active diode dimensions	$3\mu\text{m} \times 3\mu\text{m}$
die dimensions	$3.750 \times 4.050 \text{ mm}^2$	reset transistor leakage current	24aA
fabrication process	AMS CMOS 0.6 CUP (3M+2P, p-epi)	active diode leakage current	2.9fA
pixel structure	3-transistor active pixel	conversion gain	1 diode pixel – $16\mu\text{V}/e^-$ 4 diodes pixel – $6\mu\text{V}/e^-$
number of active pixels	4 arrays 64×64 pixels each	noise	1 diode = $49 e^-$ ENC= $11e^-$, kTC= $47e^-$ 4 diodes = $73 e^-$ ENC= $25e^-$, kTC = $68 e^-$
pixel dimensions	$20\mu\text{m} \times 20\mu\text{m}$	operation speed	up to 10MHz

Table 3. Basic parameters of MIMOSA prototype.

IV. EXPERIMENTAL TESTS RESULTS

The prototype chip MIMOSA has been extensively tested using high energy minimum ionising particles (15 GeV/c pions from CERN PS) and soft X-rays (5.9 keV from ^{55}Fe source). The readout has been done using VME Flash ADC unit (VFAS) designed and manufactured at LEPSI. The VFAS unit is a general-purpose ADC converter having 2 analog inputs per VME module, 12-bits resolution, 40 MHz maximum conversion rate and a memory of 8192 samples/channel. Apart of analog inputs, the module provides several digital I/O ports driven by the XILINX based, programmable logic unit. Two of these ports have been used as MIMOSA drivers, providing CLOCK and RESET signals. Two others received control pulses from the chip (CHIP-SYNCHRO and LINE-SYNCHRO) for timing verification. Another two I/O provide handling of a trigger signal from scintillation detectors and synchronisation with high-resolution reference telescope equipped with silicon strip detectors [9]. For this test purpose, the VFAS acquisition module memory has been organised as a circular buffer, with enough space to store two consecutive MIMOSA frames. Following reset pulse, MIMOSA output is constantly sampled at the readout frequency. When readout of the first frame is finished, the trigger receiver is activated. After that, data acquisition is continuing for another 4096 samples and then it is stopped. Thanks to this readout method an image of the entire array with its state before and after particle arrival becomes available for the analysis. Approach taking advantage of the trigger is obviously possible only in the case of MIPs. During the tests with X-ray photons, where there is no trigger available, the acquisition is stopped immediately after the second frame. The useful signal is calculated as the difference (for each pixel) between second and first frame. Such a signal calculation corresponds to Correlated Double Sampling (CDS) with the sampling time difference (charge integration) equal to the readout time of one full frame. The readout frequency was set to 2.5 MHz, so the charge integration time is 1.6 ms. The dominant noise source (kTC) is therefore suppressed and individual array pixel

dispersions (except the leakage current) automatically compensated. To reduce FPN most of tests have been done at low temperature (about -20°C), allowing also comfortably long time ($>100\text{ms}$) between reset and random trigger arrival.

In order to measure the basic prototype parameters, the 5.9 keV photons have been used as an excitation source. Each photon generates a charge of 1640 electrons, so the measurement of X-ray peak position should allow (supposing 100% efficient charge collection) the calculation of total conversion gain. Then the individual pixel equivalent noise charge (ENC) can be estimated from the variation around the pedestal after CDS. Because CDS value is a result of two independent measurements, thus actual pixel ENC (other than kTC) is equal to the calculated rms value for one pixel divided by square root of 2. Pedestal value after CDS is a manifestation of the individual pixel leakage current. For the measurement of the conversion gain at the pixel level, it was assumed that the total charge generated by each 5.9 keV photon is totally collected within a cluster of 25 pixels (5x5 cluster) around photon impact point. Central pixel is identified as the highest signal in a cluster. Table 4 shows total charge collected (5.9 keV photon peak position) as a function of cluster's size. Relatively small difference between charge collected on the 3x3 cluster with the respect to the 5x5 cluster justifies above assumption. It is also consistent with our device simulation results. Figure 10 shows the distribution of the 3x3 cluster signal sum for three major types of pixels: single-diode, four diode and single-diode with edgeless (supposed radiation-tolerant) reset transistor.

Two plots on this figure show results of measurements done at low temperature (-20°C), the third plot depicts data taken at room temperature. The summary of calibration measurements is given in Table 5.

Cluster size	1 pixel	3x3 pixels	5x5 pixels
Total charge : single-diode	10.5	33.5	37.5
Total charge : 4-diode	9.5	16.5	16.5

Table 4. Cluster total charge (in ADC units) measured for X-ray photons as a function of a cluster size

Pixel geometry	Conversion gain [$\mu\text{V}/\text{e}$]	ENC (except kTC) [e]	Leakage current [fA] ($-20^{\circ}\text{C}/20^{\circ}\text{C}$)
Single diode	15.0	15	1.3 / 27
4-diode	6.1	31	2.7 / 30

Table 5. Measured performance of MIMOSA prototype

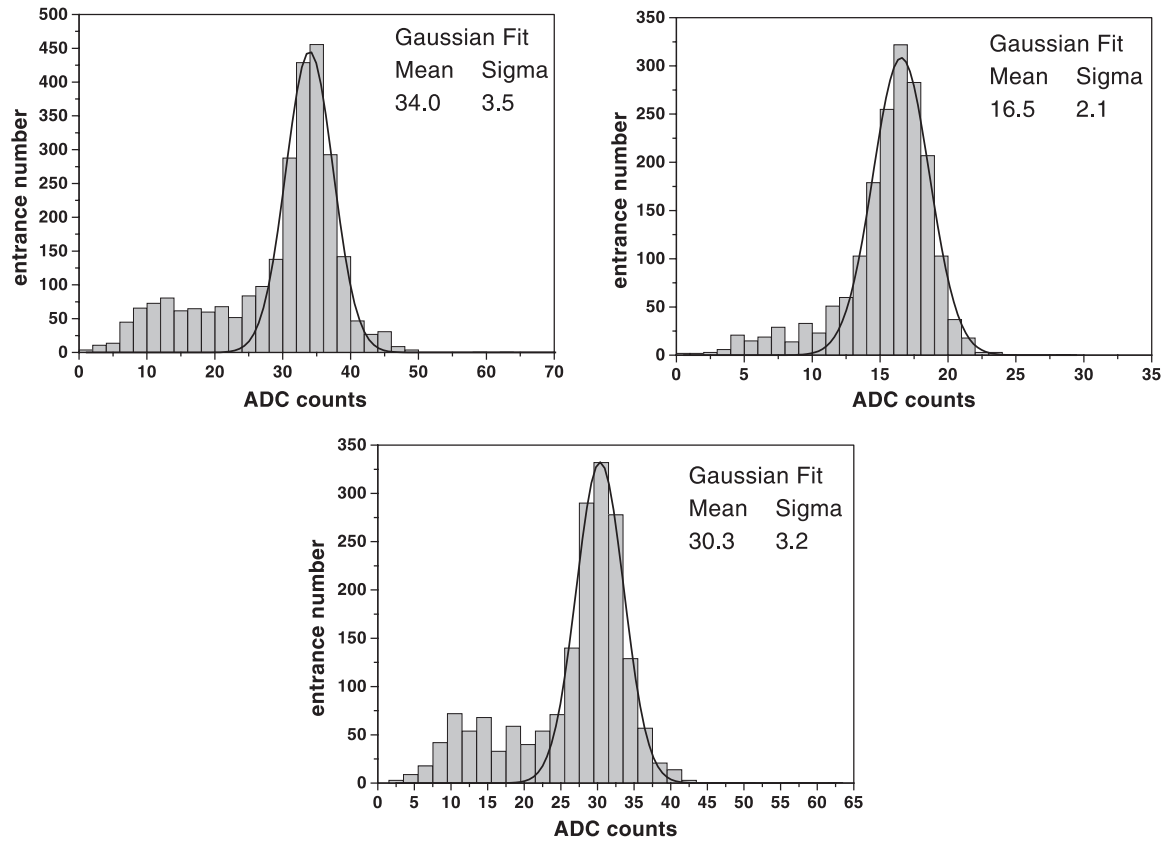


Figure 10. Calibration results with 5.9 keV X-ray photons for three major pixel structures: single-diode (upper left), four-diode (upper right) and edgeless reset transistor type, single-diode structure (below). The last measurement has been done at room temperature.

In order to test performance of MIPs tracking of MIMOSA beam tests using 15 GeV/c pions from CERN PS accelerator has been done. Figure 11 shows display of two typical events after CDS. Very preliminary analysis done by an on-line program indicates signal-to-noise ratio of about 40. S/N is defined in this case as the ratio between total charge collected in a cluster around the impact position and an individual pixel noise. Total charge collected is about 1000 electrons in agreement with the device simulations. Detailed analysis of the beam tests, including a measurement of detection efficiency and spatial resolution is currently under way, and the results will be published elsewhere.

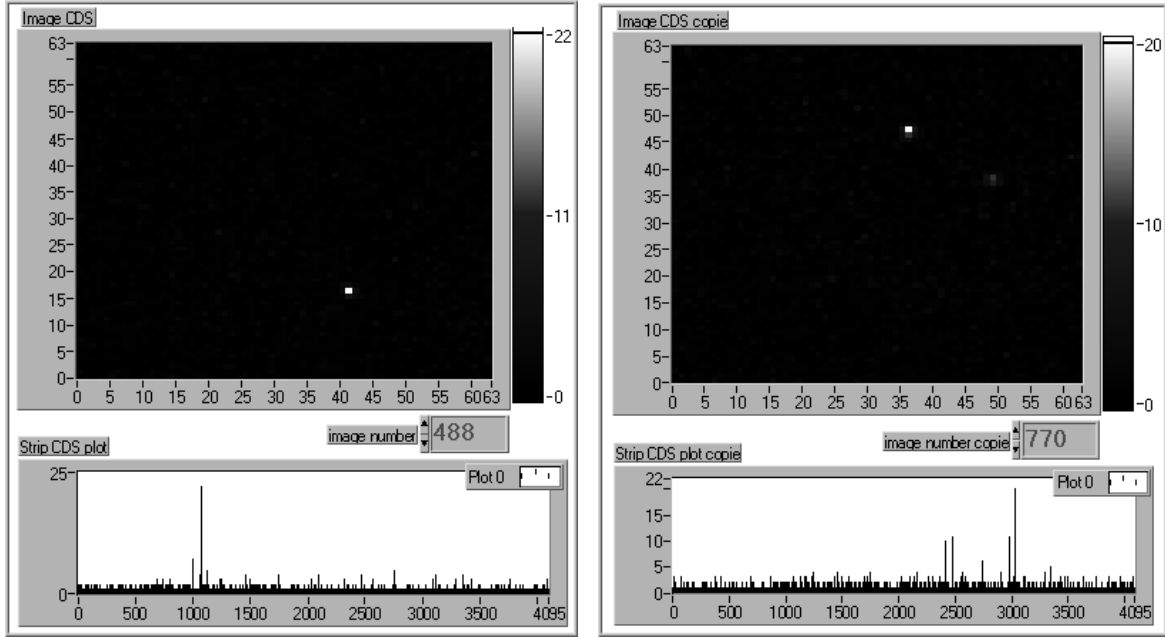


Figure 11. Two typical raw events of MIP detection with a single particle (left) and two particles (right) hitting the array. Upper plot shows 2-D event display; lower is a serial output of the pixel charge after CDS.

V. CONCLUSION

In this paper we presented a novel Monolithic Active Pixel Sensor (MAPS) for the detection of charged particles. As APS used in visible light applications, it is manufactured in a standard VLSI CMOS technology. The detector with all the front-end and the control electronics integrated on a single chip is an attractive feature with respect to other solutions like Hybrid Active Pixel Sensors or CCD's. The design is relatively straightforward and other functionalities can be integrated on a chip.

In order to achieve high charge collection efficiency for charged particle detection, special pixel architecture is put forward. It makes use of widely used cross-section of present CMOS technology, where twin wells are made in a slightly doped p-type epitaxial layer grown on the p⁺⁺ substrate. If the n-well / p-epi diode is used as the collecting element, all the front-end electronics can be integrated in a p-well. The impinging radiation creates charge passing through the device and particularly in the partially depleted thick epitaxial layer. Because of the difference in doping levels, a potential barrier is present at the boundaries between the epitaxial layer on one side and the p-well or the p-substrate on the other. By diffusion and drift, the excess electrons in the epitaxial layer move towards the n-well / p-epi diode where they are collected.

We have designed a prototype device (MIMOSA = Minimum Ionising particle MOS Active pixel sensor) to test the effectiveness of this concept. This prototype consists of 4 arrays of 64 by 64 elements at 20 μm pitch. In each array a different pixel design has been implemented. Two different semiconductor device simulators (ToSCA and ISE-TCAD) have been used to calculate the charge transport performances of the structure, like collection time and charge spread. The collection time is relatively fast (in the order of 100 ns) and the charge is confined to a few pixels, the amount of spread depends on the pixel geometry. The prototype has been tested with MIPs (15 GeV/c pions) as well as with low energy X-rays from a ^{55}Fe source. The experimental results are in good agreement with the simulation and a signal-over-noise ratio of the order of 40 is obtained in both cases. A detailed analysis of the MIP data is under way and will be presented elsewhere.

The characteristics and performances of this device make it very attractive for vertex detector in high energy physics, as well as in many other applications requiring imaging of charged particles, such as beta imaging, visible light single photon imaging (using the Hybrid Photon Detector approach) or high precision slow neutron imaging.

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